

REMARKS

The Office Action of April 8, 2005, has been received and its contents carefully considered. Applicants respectfully request reconsideration and allowance of the above-captioned application.

It was noted that Figure 1 has a typographical error in that switches "s2a, s4a, and s6a" should have been -- s2b, s4b, s6b--, respectively. Applicants have submitted a replacement drawing with that amendment to Figure 1. No new matter has been added. Applicants respectfully request that the replacement drawing be acknowledged in any following correspondence.

Claims 1-32 are pending in the application. Claims 6-9, 11-17, 20-26, 28-30 and 32 have been withdrawn. Claims 1-5, 10, 18, 19, 27 and 31 have been rejected. Applicants have canceled claims 3 and 4 and have added new claims 33-36.

Claims 1, 2, 4, 5 and 10 have been rejected under 35 U.S.C. §102(e) as being anticipated by Matsushima et al. (U.S. Patent No. 6,396,468).

Claim 27 has been rejected under 35 U.S.C. §102(e) as anticipated by Yonemoto et al. (U.S. Patent No. 6,166,769).

Claim 31 has been rejected under 35 U.S.C. §102(b) as anticipated by Hayashi et al. (U.S. Patent No. 5,818,413).

Claims 18 and 19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Matsushima in view of Hayashi (U.S. Patent No. 5,818,413).

Applicants have currently amended claims 1, 18, 27 and 31 to recite, among other features, a transfer stage comprising one switch and one buffer.

For a claim to be anticipated each and every element in the claim must be found, expressly or inherently in a single prior art reference. *Verdegaal Bros. v. Union Oil of California*, 814 F.2d 628, 531, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

With regard to the rejections of claims 1, 2, 4, 5, 10, 27 and 31, none of the cited references discloses a transfer stage each comprising only one switch and one buffer. None of the cited references discloses an output circuit which comprises a sequence of AND gates and logically combines the output signals of the transfer stages with another signal to generate scanning pulses.

Matsushima et al. discloses that gate driver 3 of the liquid crystal display device comprises shift register 3a. However, as stated in the Office Action, Matsushima et al. fails to explicitly disclose the gate driver 3 including only one switch and one buffer.

Yonemoto et al. discloses that the horizontal scanning circuit has a plurality of cascaded $\frac{1}{2}$ shift registers 151-1 to 151-6. The $\frac{1}{2}$ shift registers 151-1 to 151-6 are logically combined with each other (See Fig. 15). However, the construction of each shift register shown in Fig. 16 differs from the claimed transfer stage which comprises only one switch and one buffer. Further, Yonemoto et al. does not disclose an AND circuit which logically combines output signals of the transfer stages with another signal to generate scanning pulses. The $\frac{1}{2}$ shift registers of Yonemoto et al. are combined through NAND element 154 and NOR element 156.

One of the three criteria for establishing a *prima facie* case of obviousness is that the cited references must suggest or teach all of the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991).

With regard to the rejection of claims 18 and 19, although Hayashi et al. discloses that vertical-scanning circuit 1 of the display apparatus includes a shift register 3, the shift register 3 comprises multiple stages of D flip-flops (See column 5, lines 32 to 36), which are not transfer stages comprising one switch and one buffer as recited in claim 18.

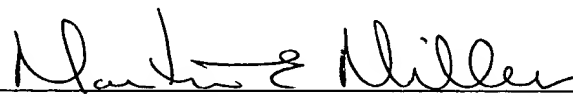
In light of the above arguments and amendments to the claims, it is respectfully submitted that claims 1-5, 10, 18, 19, 27, 31 and 33-36 are in condition for allowance.

Should any questions arise in connection with this application, or should the Examiner believe a telephone conference would be helpful in resolving any remaining issues pertaining to this application, the undersigned respectfully requests that he be contacted at the number indicated below.

Respectfully submitted,

BUCHANAN INGERSOLL PC

Date: October 6, 2005

By: 
Martin E. Miller
Registration No. 56,022

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

AMENDMENT TO THE DRAWINGS:

Figure 1 has been amended to correct a typographical error in that switches "s2a, s4a, and s6a" should have been -- s2b, s4b, s6b--, respectively. No new matter has been added. A replacement sheet with amended Figure 1 and original Figure 2 is attached.